VR Noise Analysis and Reduction in Printed Circuit Board Designs

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Abstract—Noise caused by switching voltage regulator (VR noise) can have a big impact on system signal / power performance, leading to signal integrity (SI) / power integrity (PI) issues. This paper introduces systematic ways of reducing VR noise as well as VR noise analysis methods. And a real design case with VR noise issue is shared with simulation and measurement results.

Keywords—voltage regulator noise; noise reduction; snubber circuit; noise coupling; defensive circuit

I. INTRODUCTION

Switching VR is widely used in today’s electronic designs because of their superior efficiency. And buck converter is the most popular switching VR solution in server printed circuit board (PCB) designs, which steps incoming power supply voltage like 12V down to whatever power voltage needed [1]. Fig. 1 shows a simplified buck switching converter. With the control of pulse width modulator (PWM), upper side FET (UFET) and lower side FET (LFET) switch on and off alternately to provide continuous current flow to the loadings.

While it has higher efficiency compared with linear VR, switching VR also brings some challenges due to its characteristic of fast changing voltages (dv/dt) and fast changing current (di/dt). EMI problems caused by switching VR have been widely studied [2-4]. And there are also some studies on impact of VR noise on SI [5-8] in recent years.

However, there are limited discussions on how to reduce VR noise to acceptable range in practical designs, especially in high-density boards where keeping signals far away from VR area is hard to realize.

This paper introduces VR noise analysis and reduction methods in PCB designs. In section II, different levels of VR noise analysis methodologies are listed. In section III, methods of reducing VR noise at source and at receiver as well as controlling coupling path are introduced. In section IV, a real design case with VR noise issue is analyzed and noise reduction solution is offered after finding root-cause. And a summary is provided in section V.

II. VR NOISE ANALYSIS

Accurate VR noise analysis is co-simulation (co-sim) of VR/PI/SI, which is even more complicated than normal SI/PI co-sim. However, in many cases, less accurate simulation result is also acceptable. For example, check possible VR noise coupling path for (1) optimizing layout before PCB tape-out (TO) (2) root cause and finding solution during debug.

Different levels of VR noise analysis can be used in different cases according to user’s requirement. As normal, the more accurate result is expected, the more efforts are needed.

The simplest way of VR noise analysis is to replace switching VR by simple noise source on related VR net(s), like phase, UFET node (refer to Fig.1) etc. and then do normal SI / PI analysis with 2.5D or 3D electromagnetic (EM) field simulation tools. This is usually used for quick check of noise coupling path in PCB layout, in which how VR works is not the key point. If measurement result is available, voltage / current source can be added according to the waveform. If it’s before TO, a simple sine source can be added according to [6] to imitate the high frequency resonance at phase node as VR noise source.

The second level of VR analysis is to use behavior models as VR source. [7-8] introduce a method of building behavior FET models. This method shows some impacts of switching
FET and connects VR FET with signals / powers in the simulation.

The most accurate and complicated way is to combine full switching VR analysis with SI/PI analysis. It can be a two-stage simulation: do full switching VR analysis [9] first to get waveforms of VR nets and then add them as source in full board SI / PI analysis.

User can select different simulation method per requirement at different design stage.

III. VR NOISE REDUCTION

Like other signal / power distributions, VR noise channel consists of three components: source, path and receiver. As shown in Fig.2, on board switching VR is the noise source; layout on PCB offers the coupling path from VR to signal / power rails; and receiver devices connecting the noisy signal / power serves as the noise receiver.

In most cases, keeping signal / power rails far away from switching VR area is the first option to avoid VR noise. That is, we try to minimize the coupling path during layout. However, PCB routing density has continuously been increasing with more features and/or smaller form factors needed. And on the other hand, with the increasing complexity of electronic designs, there are more different power rails on a PCB which results in more switching VRs on a limited board. So it is becoming harder and harder to always keep signal / power away from VR area.

As the other two components of VR noise channel, doing noise-aware VR design and using defensive circuit at receiver can also help reduce VR noise.

A. Reduce VR noise – efforts at source

Traditionally, VR engineer focuses on VR performance only during VR design, not taking VR impact on other signals / powers into account. With higher density routing, doing noise-aware VR design is becoming more and more important to help control VR noise since switching VR is the noise source.

There are generally two ways to control noise source. The first one is to limit the noise source area and the other is to weaken the noise source.

Some VR nets are noisy by nature according to the working mechanism of switching VR, like phase, UFET node, boot, gate, snubber etc. Controlling routing area of these nets, especially phase / UFET node which are usually routed as shape, can surely contribute to controlling VR noise. VR engineer and SI engineer can co-work on the routing optimization. For example, if loading of a certain phase is not big, avoiding routing phase shape on inner layers can be a good option in high-routing-density products because using inner layer for phase / UFET node shapes ‘wastes’ signal routing place on adjacent layers (signals are highly recommended not to be routed on adjacent layers of the noisy shapes due to big noise coupling). Besides, good placement of VR circuits can also help control noise. For example, putting input capacitor(s) on the same side of UFET can decrease the number of high di/dt vias on UFET node and those noisy vias may impact signal/power vias even >100mils away [8].

There are detailed discussions of VR noise source formation mechanism in [6]. Adding series resistor at FET gate can weaken the resonance at phase. And using RC-snubber circuit can also attenuate the oscillation at phase node. Both methods weaken the noise source. However, they may have some impact on VR efficiency. Designer needs to balance between VR performance and system SI / PI performance.

Table 1 below is the measurement result of snubber impact on one switching VR. It can be seen that the RC-snubber effectively attenuate the resonance on phase and its impact on VR efficiency is slight (data in table below is for full load).

<table>
<thead>
<tr>
<th>Snubber R (Ohm)</th>
<th>Snubber C (nF)</th>
<th>Phase Max voltage (V)</th>
<th>VR efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>unstuffed*</td>
<td>unstuffed</td>
<td>17.9</td>
<td>84.15 %</td>
</tr>
<tr>
<td>1</td>
<td>3.3</td>
<td>14.41</td>
<td>83.98 %</td>
</tr>
</tbody>
</table>

B. Reduce VR noise – efforts at channel path

There are also two ways of reducing VR noise on the channel path (signal/power routing on PCB). The first one is to try to cut noise coupling path from switching VR to signal / power victims. And the other one is to decrease noise of victim on their way to receiver, especially for power delivery.

There are detailed discussions of VR noise coupling mechanism in [6-8]. And the basic method of controlling noise coupling is to make spacing bigger, keeping signals / power shapes far away from the VR noisy parts, in all three dimensions. And signals / powers can be classified into different groups according to their margin allowable for noise. E.g. 3.3V signals in one group, 1V signals in another group. And net groups of smaller margin are prioritized to have bigger spacing from VR noisy nets during layout.

Capacitors can be added on the power delivery network to filter noise caught from switching VR. When noise is coupled onto a power rail, it can spread along the power shape to different parts of the board. And it’s possible to form a 2nd noise coupling, in which VR noise coupled onto power shape works as a noise source to other signals / powers referencing it. So capacitors need to be put along the power path, especially
area close to the switching VR for a timely noise-filtering if power shape cannot avoid routing near VR noisy parts.

C. Reduce VR noise – efforts at receiver

Circuit receiver has input requirement / SPEC for each signal / power pin. The thing that matters is not whether there is VR noise on signal / power at receiver or not, but whether the noise is within acceptable range or not. For example, a 400mV peak-to-peak (p-p) VR noise can mean totally different things for a 1V signal and a 3.3V signal. For 1V signal, the noise may result in signal violating the Vih / Vil SPEC, so special attention needs to be paid for this VR noise. However, for 3.3V signal, since the margin is big by nature, less worry is needed. And the VR noise can be even waived so long as signal integrity on the signal itself is good and enough margin is left.

And we can also put some defensive circuit at receiver in case noise is out of acceptable range. The first option is to add capacitor at receiver to filter noise. Care needs to be paid if signal is sensitive to rising time. Another option is to add R or RC circuit to attenuate noise energy. For example, adding RC defensive circuit at the gate of voltage isolator FET (for details, please refer to the example case in section IV). And a third option is to add bead in series at receiver pin. This can be used on some low speed critical signals, like voltage monitor trace going a long way from power rail to BMC for voltage monitoring. Fig. 3 below shows a bead’s electrical characteristics. Big resistance appears at VR noise frequency (usually around hundred-MHz) which helps damp noise energy.

D. Conclusion

VR noise is unexpected in PCB design. With efforts on any one(s) or all of the three channel components (noise source, coupling path, and receiver), it’s possible to limit VR noise level within an acceptable range even on an extremely high-density board.

IV. EXAMPLE CASE

A. Issue background

In one design, VR noise was found on system management bus (SMBus) clock and data signals. Fig.4 below shows topology of the SMBus signal. More than 1V p-p noise was found at all the four receiver ends, on both ‘0’ and ‘1’, even though there was a voltage isolator on the open-drain Xnet. Fig.5 shows the SMBus waveforms at receiver 2 and at receiver 4. Yellow curve is SMBus clock signal while pink curve is SMBus data signal.
B. VR Noise Analysis

Noise appeared on the signals periodically around every 3.3us. This led to suspect of CPU VR as noise source, whose switching frequency (Fsw) was 300KHz. And this was proved by measurement result, as shown in Fig.6. Noise on SMBus occurred on the rising / falling edge of the CPU VR Phase. And it also matched the appearance of the more than 2V p-p noise on CPU VR UFET node caused by UFET switching-on-and-off. However, there was no direct coupling path found between CPU VR and traces of those SMBus branches. Both SMBus clock and SMBus data signals were away from the CPU VR noisy parts, including components, phase shapes, UFET node shapes etc. And there was no noise found on other signals routed adjacent to the SMBus branches.

Fig.8 shows the p3v3 waveform caught at FET gate (blue curve) together with the SMBus signal, indicating good match of noise appearance between the two.

C. VR Noise Reduction

After all the analysis above, root cause of the SMBus VR noise was clear: (1) noise path was CPU VR switching ➔ noise on UFET node ➔ p3v3 shape ➔ FET (voltage isolator) gate ➔ FET source / drain which connected SMBus branches to different devices; (2) poor capacitor placement on p3v3, which failed to filter the noise caught from VR UFET node; (3) no defensive circuit at FET gate, which missed the final chance of filtering the noise before it went into signals.

With root cause clear, it was time to work out solutions to reduce the VR noise. Adjusting p3v3 or UFET node shapes routing to avoid direct overlapping could be a thorough way to cut noise coupling path. However, it would cause a big layout change on the new PCB Fab, which was unexpected. And we also did not want to adjust VR designs. So solution search was focused on root cause 2 and 3.

For root cause 2, adding capacitors on p3v3 along its routing path could effectively reduce noise on the power rail. For simplicity, a noise source imitating UFET node measurement waveform was added onto the UFET shape where UFET connected as the noise source and noise level at
FET gate (p3v3) was checked. Simulation result showed that noise at FET gate reduced from 2V p-p to 0.7v p-p after adding two 0.1u capacitors at position a / b shown in Fig.10 below.

Figure 11  p3v3 noise reduction at FET gate by adding two capacitors

For root cause 3, adding a defensive resistor or RC circuit at FET gate (Fig. 11) can effectively damp the noise. And the defensive circuit has little impact on signal fall time. Simulation result showed noise level at FET drain reduced from 1.5V p-p to almost no noise after adding a 1k Ohm RES at FET gate (Fig. 12). And measurement result also verified the RES contribution (Fig.13).

As a final solution, eight 0.1uF capacitors were added along p3v3 shape path and RC (R=1kOhm, C=1nF) was added at the FET gate on the new PCB fab. And SMBus VR noise disappeared. The problem was solved.

Figure 12  Add RES at FET gate

Figure 13  Noise reduction with RES

D. Learnings

From this case, we can learn several things:

1) VR Noise on signal can be a 2nd pollution from noisy parts impacted by VR, e.g. switching VR → power → signal. And noise can be transferred through circuit as well as physical coupling.

2) Routing plan should be optimized in early layout stage, especially for VR noisy parts / shapes. If possible, try to have VR noisy shapes isolated from other layers by GND.

3) Pay attention to capacitor placement on power rail – not only close to device pins but also on the whole power delivery network.

4) Defensive circuit at possible noise-existing positions can help control noise, like RC circuit at voltage isolator FET gate.

V. SUMMARY

This paper introduces VR noise analysis and reduction methods in PCB designs. Different levels of VR noise analysis methodologies are listed. And methods of reducing VR noise at system level, including the three channel components (source, path and receiver), are introduced. With efforts on any one(s) or all of the three channel components, it’s possible to limit VR noise level within an acceptable range even on an extreme high-density board.

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References


