On-chip Design Techniques for Reducing Power Supply Noise Effects on ADC with Chip-PCB Hierarchical Structure

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***Abstract*—In this paper, we propose the on-chip design techniques for controlling Power Supply Noise (PSN) effects on Analog-to-Digital Converter (ADC) with chip-Printed Circuit Board (PCB) hierarchical structure interconnected by bonding wires. There are two steps for explaining the proposed design technique. First, we explain what the PSN coupling path is on ADC. The PSN will couple from noise source to noise victim via power distribution network and circuit path. Second, we propose how we can reduce the noise coupling effects. The comparator is essential circuit to ADC and most sensitive circuit to PSN in ADC. Therefore, it is important to reduce the noise coupling effects on comparator for designing ADC which is non-sensitive to PSN. The comparator has two input nodes, and the differential voltage between two input nodes affect to ADC output. The impedance imbalance between two comparator inputs is the reason why the comparator is sensitive to PSN. So, the technique which is for balancing two input impedance is important to reduce PSN effects. We consider chip-PCB components to estimate two input impedance, because the two input impedances are affected by chip-PCB hierarchical structure. If we control the impedance of each input, we can design the ADC which is non-sensitive to PSN at the targeted frequency. We demonstrate the proposed technique based on simulation by PSN whose frequency swept from 1MHz to 3GHz.**

I. INTRODUCTION

High density and capability trend let recent semiconductor systems be mixed-mode system having both digital and analog circuit. Even though noise has increased with higher degrees of integrating, we have to fulfil high reliability on mixed-mode system. Power Supply Noise (PSN) is frequently generated noise in mixed-mode system, and the analog circuit, which is essentially included on mixed mode system, is sensitive to PSN. So, we have to consider PSN effects on mixed mode system. The Analog-to-Digital Converter (ADC), which is the representative mixed-mode system, is the targeted system in this research. The ADC is also sensitive to PSN as common mixed mode system is sensitive to PSN. For designing non-sensitive ADC to PSN, we have to analyse which part is critically sensitive to PSN, how the PSN couple from noise source to noise victim, and what design technique can be applied for reducing PSN effects.

In high speed ADC, the critically PSN sensitive circuit is comparator, because it is the block which converts from analog signal, which can be easily changed by noise, to digital signal, which is non-sensitive to noise. When the PSN affects to comparator, the analog signal can be changed and it converts to digital signals which cannot be easily modified. Therefore, the comparator is the critical noise victim to PSN. The PSN will couple from noise source to noise victim via Power Distribution Network (PDN) and circuit path. Basically, there are two methods for designing non-sensitive ADC to PSN; one is the noise decoupling techniques on the PSN coupling path, the other is the proposed technique in this paper.

There are previous studies for the noise decoupling techniques [1]. These studies propose the technique such as mounting decoupling capacitor, applying isolated PDN [2], and designing Electromagnetic Band Gap (EBG) structures [3]. However, these techniques are accompanied by the cost and size issues, and in practical field, the cost and size issues are very important to determine whether it is good design or not [4]. Therefore, it is impossible for practical design that the PSN is fully decoupled via PDN. Even though the PSN is not fully decoupled via PDN, the design has to fulfill high reliability. Consequently, it is highly needed to discover new technique which is good for cost and size issues. Therefore, we propose a new design technique for reducing PSN effects. The mechanism of the proposed method is that the same amount of PSN couple to the two inputs of comparator for effectively rejecting PSN on the differential inputs of comparator, because comparator output is affected by the differential input which is subtraction value between two inputs of comparator. The amount of PSN couple to the inputs of comparator can be controlled by the impedance of each input, and the balanced input impedance is needed to the same amount of PSN couple to the input of comparator, which means small differential noise input. For accurate estimation of impedance, we have to consider both on-chip elements and off-chip elements.

To validate the proposed technique, we use PSN effects model on ADC with chip-PCB hierarchical structure [5]. We consider PSN swept from 1MHz to 3GHz, and we conclude this technique is meaningful to reduce high frequency PSN coupling effects.

II. POWER SUPPLY NOISE COUPLING MODEL OF ADC WITH CHIP-PCB HIERARCHICAL STRUCTURE

The ADC system is sensitive to PSN [6], because ADC has comparator which is sensitive to PSN. In this chapter, we

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explain the PSN coupling paths via chip-PCB hierarchical structure and why the ADC is sensitive to PSN. Fig. 1 shows that the ADC can be affected by PSN in the mixed mode system.

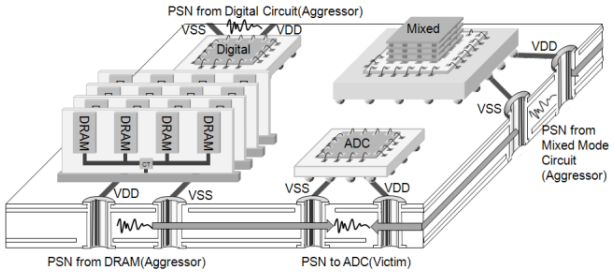

Fig. 1. The conceptual diagram of mixed mode system and the PSN coupling path from PSN source to ADC which is PSN victim.

A. PSN Path 1 from Noise Source (Port (1)) to Power/Ground of Comparator (Port (2)): Chip-PCB Hierarchical Power Distribution Network (PDN)

Fig. 2 shows the conceptual diagram and cross section view of chip-PCB hierarchical PDN. There are several PDN elements; PCB power/ground plane, bonding wires, on-chip power/ground rings, and on-chip decoupling capacitor. We use the verified modeling method [5] which is for estimating PSN coupling effects on ADC with chip-PCB hierarchical structure. This model used segmentation method for modeling of PSN coupling path on hierarchical PDN. The model can estimate PSN coupling ratio via PSN coupling path on PDN.

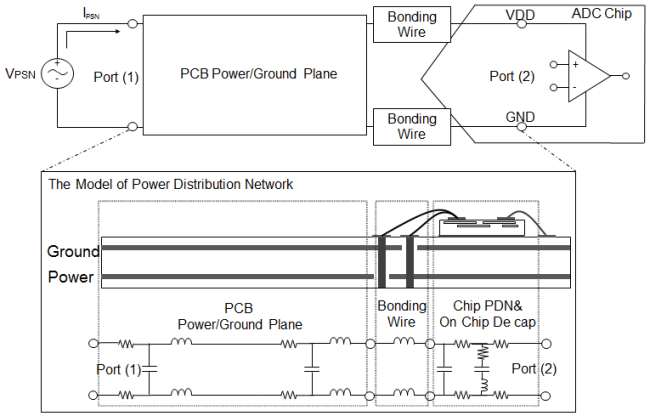

Fig. 2. The conceptual diagram and cross section view of chip-PCB hierarchical PDN. There are several PDN elements; PCB power/ground plane, bonding wires, on-chip power/ground rings, and on-chip decoupling capacitor. Each element can be modelled as lumped elements.

Fig. 3 illustrates the self-impedance, transfer-impedance, and noise coupling ratio of the chip-PCB hierarchical PDN from PSN source (Port (1)) to power/ground of comparator (Port (2)). The impedance profile has several critical characteristics, one is series resonance (f1) from the capacitance of the on-chip decoupling capacitor and inductance of the bonding wire, another is series resonance (f2) from the plane capacitance and the plane inductance, the other are the mode frequencies of cavity resonance (f3-f5) [7].

Based on these resonant points, the self-impedance curve is divided into three regions, Region1, Region2, and Region3 in Fig. 3. Initially at Region 1, the slope of the self-impedance curve is mainly affected by the capacitance of on-chip decoupling capacitor, because the capacitance of on-chip decoupling capacitor has the largest capacitance value among the model blocks of the reference design. As the frequency is over 60 MHz, the major model parameter determining the self-impedance curve is inductance of power/ground bonding wire and capacitance of PCB plane. In this region, the noise coupling ratio via PDN is gradually decreased. In Region3, the cavity resonant peaks are displayed on the self-impedance curve. Between each region, there are resonant points of model parameters, and the PSN can couple well on these series resonant points, shown on the plot of noise coupling ratio via PDN in Fig. 3.

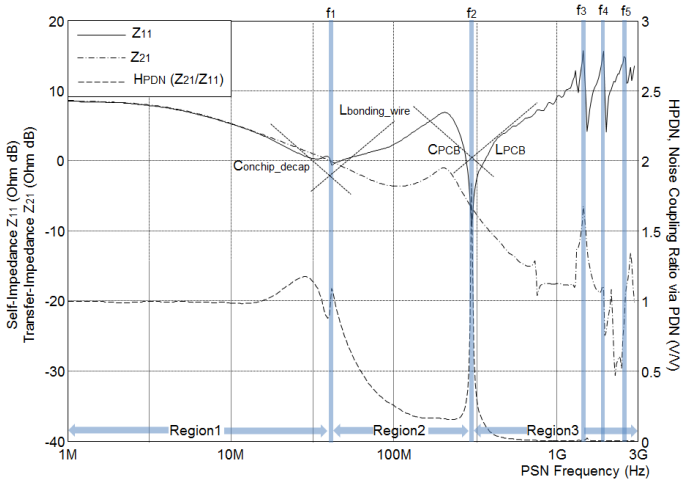

Fig. 3. Impedance profiles and noise coupling ratio between two ports; one is the port of noise source, the other is the port of the comparator power/ground

B. PSN Path 2 from Power/Ground of Comparator (Port (2)) to Differential Input of Comparator (Port (3)): Comparator which is Critical PSN Circuit Path on ADC

The differential input voltage determines the comparator outputs, which directly affect to ADC outputs. So the differential input noise is key factor to expect whether the performance of ADC is sensitive to PSN or not. Even though the noise coupling ratio via PSN Path 1 is high, the ADC is not sensitive to PSN when the noise coupling ratio via PSN Path 2 is low. Therefore, it is needed to reduce differential input noise coupled by PSN. For achieving that, the analysis of coupling ratio between power/ground of comparator and two inputs of comparator is essentially needed.

Fig. 4 shows the schematic of the comparator used in designed ADC. The voltage of Port (2) is the power/ground AC voltage of comparator, and it coupled to the voltage of Port (3), which is the differential input voltage of comparator, because of impedance imbalance between two input nodes,

one is connected to analog input and the other is connected to reference ladder. The reference ladder affect to impedance of Zref, and the signal line of PCB and signal bonding wire affect to impedance of Zin.

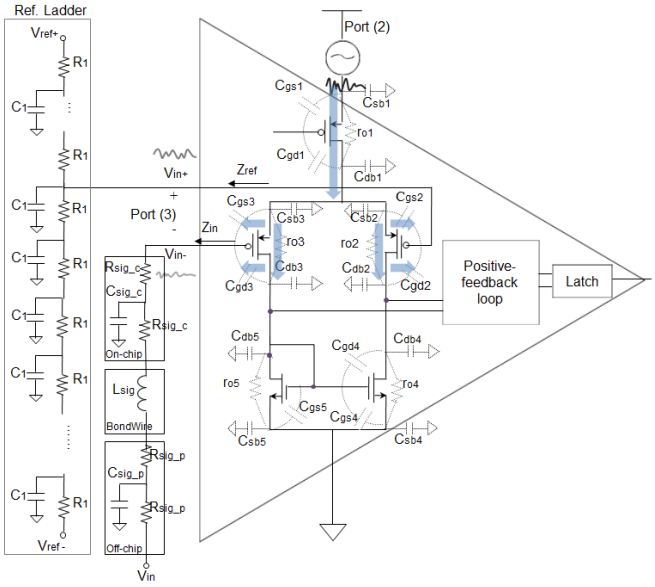

Fig. 4. Schematic of the comparator used in designed ADC. Port (2) is the power/ground AC voltage of comparator, and it coupled to the differential input voltage of comparator Port (3), because of impedance imbalance between two input ports, one is connected to analog input and the other is connected to reference ladder.

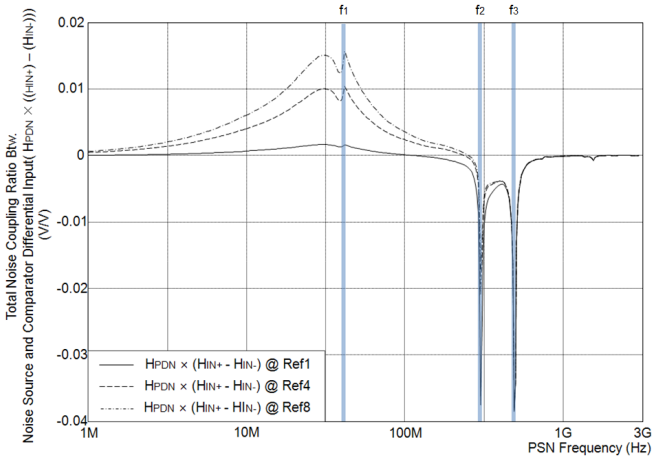

Fig. 5. The total noise coupling ratio between noise source and comparator differential input (Vin+ - Vin-).

Fig. 5 is the noise coupling ratio between noise source (Port (1)) and differential input (Vin+ - Vin-) of comparator (Port (3)) without impedance balancing for reducing PSN effects. This result is the result which is multiplied by two noise coupling ratio; one is the noise coupling ratio via hierarchical PDN, the other is the noise coupling ratio via comparator circuit. ADC generates output bits from differential input of comparator. Therefore, the high coupled differential input noise of comparator generates many error bits of ADC outputs. It is verified previous research [5]. If we reduce the differential input noise of comparator, then the ADC outputs are not affected by PSN. So, we focus on the reducing differential input noise. Now, we propose the new design method for reducing differential input noise through controlling the noise coupling ratio via comparator circuit.

III. Proposed Design Technique for Reducing PSN Coupling via Comparator Circuit

If we want to reduce the PSN effect of targeted frequency, then we can insert passive component for balancing impedance, as shown in Fig.6. This method needs three steps for designing.

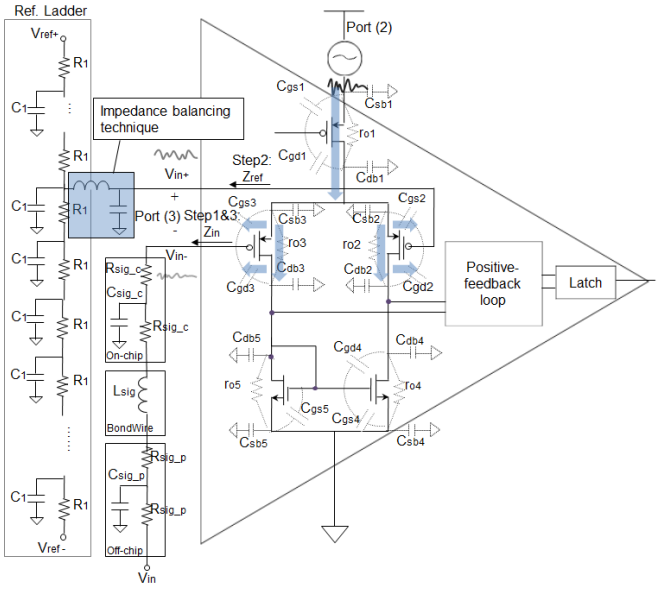

Fig. 6. Schematic of the comparator used in designed ADC with proposed impedance balancing technique for reducing high frequency PSN coupling. There are three steps for applying this proposed technique.

A. Step 1:Signal Input Impedance (Zin) Calculating at Targeted Frequency

First of all, we have to determine the targeted frequency, which is the frequency we want that PSN is not coupled well to ADC. When we determine the targeted frequency, then we can estimate the signal input impedance (Zin) of comparator at targeted frequency. The components which affect to signal input impedance is on-chip signal line, off-chip signal line, and the signal bonding wire which is connected between on-chip and off-chip signal line.

B. Step 2:Insert Impedance Components for Reference Input Impedance (Zref)

The differential input noise from PSN is affected by the balancing two comparator input impedances. The signal input

impedance (Zin), which is one of the comparator input impedances, has to be same of the impedance of reference input node (Zref) for rejecting differential input noise of comparator. So, we insert the lumped components for impedance balancing at targeted frequency. The important lumped component which we have to insert to on-chip reference ladder design is inductance, because the chip-PCB hierarchical signal line structures are connected by bonding wire modelled as an inductance.

C. *Step 3:Insert Impedance Components for Modified Signal Input Impedance (Zin)*

When the chip and PCB are fabricated, the practical impedance can be changed by parasitic terms. Therefore, more accurate impedance balancing between two inputs of comparator, we have to compensate unwanted parasitic terms. Then, we can take the ADC which is not sensitive to PSN whose frequency is same to the targeted frequency.

D. *The Noise Coupling Ratio to Differential Input of Comparator*

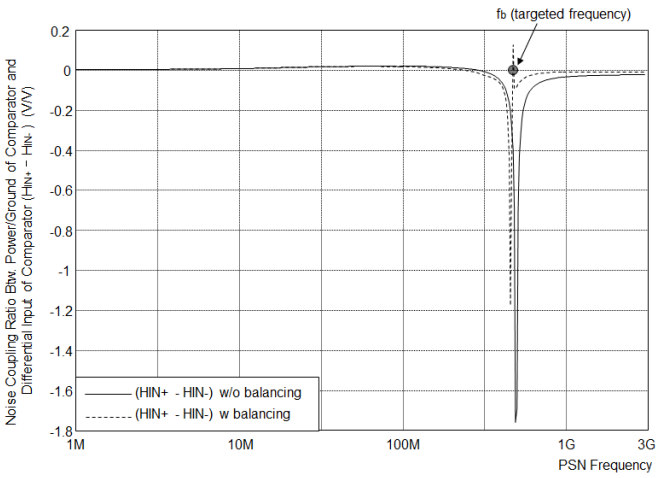

Fig. 7. The comparison result with or without impedance balancing technique about PSN coupling ratio between power/ground of comparator and the differential input of comparator. This coupling ratio is zero at targeted frequency.

In this paper, as a case study, we targeted 470 MHz PSN which is highly coupled from noise source to differential input of comparator without balancing technique. Fig.7 displays the comparison result with or without impedance matching technique about on-chip PSN coupling ratio between power/ground of comparator (Port (2)) and the differential input of comparator (Port (3)). We achieve the result that the PSN whose frequency is same to targeted frequency is not coupled to differential input of comparator, and it shows balancing technique is meaningful to reduce the PSN coupling whose frequency is over 470MHz in this case.

Fig. 8. shows the noise coupling ratio between PSN source (Port (1)) and differential input (Vin+ - Vin-) of comparator (Port (3)) with or without balancing technique. The PSN coupling ratio is zero at targeted frequency (470MHz) and reduced over 470MHz. Therefore, this technique can be applied for the PSN, which is highly generated by PSN source or which critically degrade ADC performance.

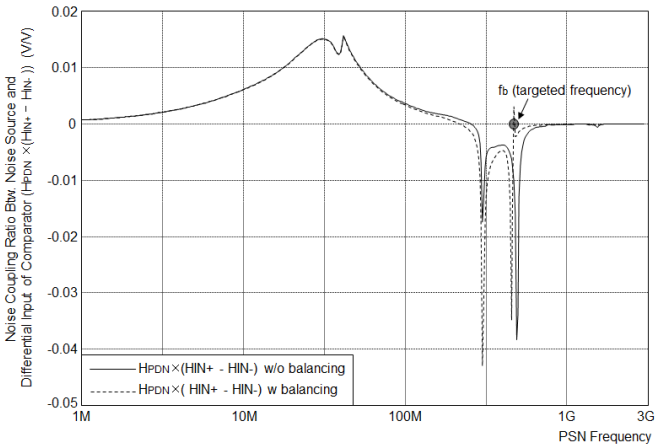

Fig. 8. The total noise coupling ratio between external noise source and comparator differential input (Vin+ - Vin-) with or without matching technique. This coupling ratio is zero at targeted frequency.

IV. Conclusion

In this paper, we proposed the new design technique for reducing PSN effects on ADC with chip-PCB hierarchical structure. The comparator is the key block to determine ADC performance, even though it is sensitive to PSN. Therefore, it is needed to reduce the PSN coupling on comparator circuit. The PSN is coupled to two inputs of comparator, and the differential value of the two inputs affect to ADC performance. So, the differential value is most important to determine ADC performance. If same amount of noise is coupled to each input from PSN, the differential input noise is zero. It is impossible to remove the differential input noise on the practical comparator design in ADC at whole frequency range, because of impedance imbalance between each input. However, if we determine the PSN whose frequency want to be not coupled well to differential input of comparator, then we can balancing two input impedance at targeted frequency. Through this proposed technique, we can design the ADC which is non-sensitive to the PSN whose frequency element is critical to circuit behaviour. We demonstrate the proposed technique based on simulation whose frequency swept from 1MHz to 3GHz.

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REFERENCES

[1] Gong, S.; Hentzell, H.; Persson, S.-T.; Hesselbom, H.; Lofstedt, B.; Hansen, M.; , "Techniques for reducing switching noise in high speed digital systems," *ASIC Conference and Exhibit, 1995., Proceedings of the Eighth Annual IEEE International* , vol., no., pp.21-24, 18-22 Sep 1995

[2] Hyunjeong Park; Jongjoo Shim; Yujeong Shim; Jeongsik Yoo; Joungho Kim; , "Experimental verification and analysis for noise isolation of analog and digital chip-package-PCB hierarchical power distribution network," *VLSI Packaging Workshop of Japan, 2008. VPWJ 2008. IEEE 9th* , vol., no., pp.73-76, 1-2 Dec. 2008

[3] Myunghoi Kim; Changwook Yoon; Kyoungchoul Koo; Chulsoon Hwang; Hajin Sung; Joungho Kim; , "Suppression of power/ground noise using meshed-planar electromagnetic bandgap (MP-EBG) structure for Ultra-Wideband (UWB) System-in-Package (SiP)," *Electromagnetic Compatibility (EMC), 2010 IEEE International Symposium on* , vol., no., pp.28-31, 25-30 July 2010

[4] Van der Plas, G.; Limaye, P.; Mercha, A.; Oprins, H.; Torregiani, C.; Thijs, S.; Linten, D.; Stucchi, M.; Guruprasad, K.; Velenis, D.; Shinichi, D.; Cherman, V.; Vandevelde, B.; Simons, V.; De Wolf, I.; Labie, R.; Perry, D.; Bronckers, S.; Minas, N.; Cupac, M.; Ruythooren, W.; Van Olmen, J.; Phommahaxay, A.; de Potter de ten Broeck, M.; Opdebeeck, A.; Rakowski, M.; De Wachter, B.; Dehan, M.; Nelis, M.; Agarwal, R.; Dehaene, W.; Travaly, Y.; Marchal, P.; Beyne, E.; , "Design issues and considerations for low-cost 3D TSV IC technology," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International* , vol., no., pp.148-149, 7-11 Feb. 2010

[5] Bumhee Bae; Yujeong Shim; Woojin Lee; Kyoungchoul Koo; Woojin Ahn; Joungho Kim; , "Hybrid modeling and analysis of power supply noise effects on analog-to-digital converter considering hierarchical PDNs," *Electrical Design of Advanced Packaging & Systems Symposium (EDAPS), 2010*

[6] Carbone, P.; Petri, D.; , "Noise sensitivity of the ADC histogram test," *Instrumentation and Measurement, IEEE Transactions on* , vol.47, no.4, pp.1001-1004, Aug 1998

[7] Beyene, W.; Chuck Yuan; Joong-Ho Kim; Swaminathan, M.; , "Modeling and analysis of power distribution networks for gigabit applications," *Quality Electronic Design, 2003. Proceedings. Fourth International Symposium on* , vol., no., pp. 235- 240, 24-26 March 2003